Logic Definitions

Literal	Boolean variable
Minterm	Conjunction of **all** variables complemented or otherwise
DNF	Disjunction of all minterms
Maxterm	Disjunction of **all** variables complemented or otherwise
CNF	Conjunction of all maxterms
Cover	Term covers a minterm if that minterm is part of the tem
Implicant	A product term T is an implicant of a formula G iif G is true for all input combinations that make T true
Prime Implicant	A product term T is a prime implicant of a formula G iif T is an implicant of G and no proper subterm of T is an implicant of G
Essential Term	A prime implicant which covers a minterm that no other prime implicant covers
Covering Set	A minimum set of prime implicants which includes all essential terms
Static Hazard	Output glitches but returns to the original level
Dynamic Hazard	Output changes state but glitches during the change

Circuits

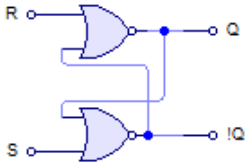
Fast Carry Adder

$$g_n = a_n.b_n,\ p_n = a_n + b_n$$

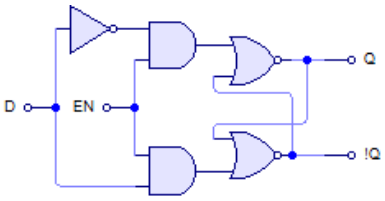
$$c_{n+1} = g_n + p_n.c_n \Rightarrow$$

$$c_{n+2} = (g_{n+1} + p_{n+1}.g_n) + (p_{n+1}.p_n).c_n$$

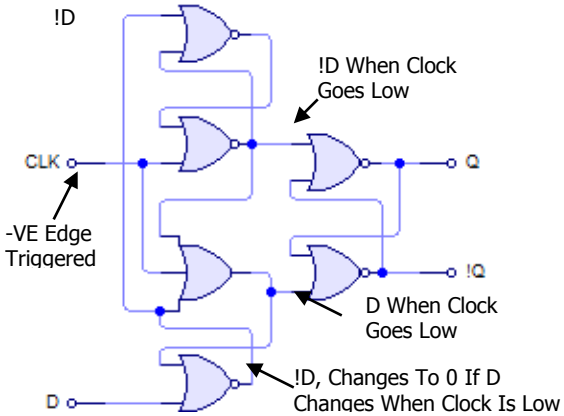
RS Latch



D Latch



D Flip Flop



Or alternatively two clocked RS latches in series.

Obscure Sync. Flip Flops

J	K	Q'
0	0	Q
0	1	0
1	0	1
1	1	!Q

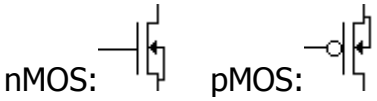
T	Q'
0	Q
1	!Q

State Machines

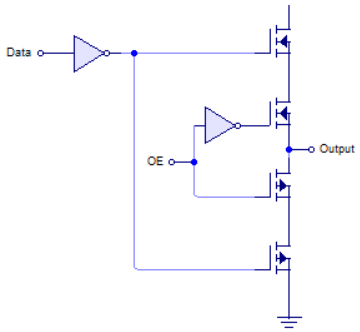
Finite State Machine	Deterministic circuit producing outputs dependent on its internal state and external inputs
States	Set of internal memorized values, shown as circles on diagrams
Inputs	External stimulus to the machine, shown as arcs on diagrams
Outputs	Results from a FSM, associated with a state (Moore) or a function of the state and inputs (Mealy)
Start Up State	Reset or self starting
Encoding	Shift, sequential, sliding, one hot

Building Gates From Transistors

FETs



Tristate Buffer



Programmable Logic Devices

ROM	Implements table lookup $O(m*2^n)$
PAL	Selectively remove connections in NOT, AND and OR planes, scale with number of terms not states